In the Claims:

1-11. (canceled)

12. (amended) A process of testing an integrated circuit comprising:

A. applying stimulus test signals to input pads of the integrated circuit;

B. conveying the applied stimulus test signals to core circuits in the integrated circuit;

C. producing core test response output signals from the core circuits in response to the stimulus test signals;

D. applying expected response test signals to output pads of the integrated circuit; and

E. comparing on the integrated circuit the core test response output signals to the expected response test signals ~~on the integrated circuit~~ received on the output pads to produce a pass/fail signal.

13. (previously presented) The process of claim 12 including switching output buffer circuitry from output circuitry to input circuitry to accept the applied expected response test signals.

14. (previously presented) The process of claim 12 including applying stimulus test signals to input pads of plural integrated circuits in parallel.

15. (previously presented) The process of claim 12 including applying expected response test signals to output pads of plural integrated circuits in parallel.